## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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TITLE: METHOD AND APPARATUS FOR THERMAL SENSITIVITY BASED ON DYNAMIC POWER CONTROL

ART UNIT: 2116

EXAMINER: Tse W. CHEN

**Mail Stop Appeal Brief - Patents**
Commissioner for Patents
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## REPLY BRIEF

SIR:

In response to the Examiner's Answer mailed February 2, 2006, this reply brief is respectfully submitted.

## Remarks

The following remarks address the Examiner's comments in the "Response to Argument" portion of the Examiner's Answer.

The claims on appeal relate to thermal throttling in a processor. When the processor approaches temperature limits, its clock frequency is reduced to allow it to cool. A performance demanding level input may be used to determine a rate of the frequency reduction. A "performance demanding level input" in a processor, by its terms, is an input that relates to a level of performance of the processor in accordance with demand. That is, if the processor approaches a

temperature limit but nevertheless high performance is demanded, the performance demanding level input may assert a value that causes the frequency reduction to be less aggressive. If, on the other hand, the processor approaches a temperature limit but high performance is not demanded, the performance demanding level input may assert a value that causes the frequency reduction to be more aggressive.

The Examiner alleges that McDermott et al. (McDermott) "teaches the concept of a **performance demanding level input** ... " (emphasis in original) (Examiner's Answer, page 9, item 26, line 15). This is in error. McDermott does not even remotely suggest an input that relates to a level of demand for performance in a processor. The signals LVL1, LVL2 disclosed in McDermott and cited by the Examiner as corresponding to the claimed performance demanding level input reflect, not a level of demand for performance in a processor, but a *phase relationship* between an input clock and feedback in a PLL circuit.

Still less does McDermott suggest an input that determines a rate of frequency reduction in a processor in accordance with a level of demand for performance. Indeed, the sole purpose of McDermott's invention is to assure that the frequency of the system clock does *not* change. Specifically, the LVL1, LVL2 signals are designed to cause the PLL's output, which is the CPU's clock in McDermott's system (see FIG. 1 and col. 4, lines 40-45), to converge in frequency with an input clock more swiftly or less swiftly, depending on how much the PLL's output frequency diverges from that of the input clock. When the PLL is stable, meaning that its output is well-synchronized with the input clock, LVL1 and LVL2 are low and the PLL output frequency changes slowly. When the PLL output frequency and input clock frequency begin to diverge significantly, LVL1 and LVL2 go high to cause the output frequency to change faster, thus correcting the divergence more quickly. See, e.g., McDermott at col. 9, lines 19-30.

Thus, LVL1 and LVL2 are elements in a synchronization mechanism whose purpose is maintain stability of an output clock, not to change it. Moreover, to this end the LVL1 and LVL2 signals are slaved or reciprocally tied by feedback connections and a system of logic gates to the input and output of the synchronization mechanism (the PLL). See, e.g., FIG. 3 of McDermott. Therefore, the LVL1 and LVL2 signals cannot change the rate of frequency reduction of the PLL output based on anything but the PLL output itself, and the input clock. This arrangement in no way suggests determining a rate of frequency reduction based on a demand for performance at a given level in a processor as called for in the claims on appeal.

The Examiner further contends:

> "One of ordinary skill in the art would be motivated by [the combined teachings of Georgiou et al. and McDermott] to implement the **performance demanding level input involved in frequency reduction based on temperature** in order to have better control of frequency changes via a performance demanding level input ... for systems such as Georgiou's that is involved in frequency reduction based on temperature changes."

(Examiner's Answer, page 10, lines 2-6; emphasis in original.) This is further error. As discussed above, McDermott relates to frequency *stability*, not frequency *change*. The Examiner concedes as much, quoting McDermott: "McDermott 'provide[s] a fully integrated charge pump PLL having a fast response time to input frequency changes as well as highly stable behavior ...'." (Examiner's Answer, page 10, lines 21-22 to page 11, line 1). The person of ordinary skill, seeking to reduce clock frequency in accordance with a level of demand for processor performance, would not look to a reference describing an invention whose sole purpose is to prevent clock frequency change. The Examiner has not shown any motivation to combine Georgiou et al. and McDermott

More importantly, as also discussed earlier, McDermott contains no suggestion whatever of a performance demanding level input – the Examiner has made no logical connection between the LVL1 and LVL2 signals of McDermott and an input that determines a rate of frequency reduction based on a demand level for processor performance. The Examiner applies the overly-broad concept of "control of frequency" in a strained effort to bring the claims on appeal within the sphere of McDermott. But control of frequency by the performance demanding level input of the claims on appeal is to *change* a clock frequency; control of frequency by the LVL1 and LVL2 signals of McDermott is to *prevent* a change in clock frequency.

Note is further taken of the Examiner's comments on page 10, lines 9-12:

> "Firstly, Examiner notes Appellant's concession that McDermott does teach the synchronization of a PLL and submits that better control of frequency changes in any system [i.e., including a system involved in frequency reduction based on temperature changes as taught by Georgiou] requires an effective synchronization scheme in order to function properly."

This statement is unclear and its conclusion unfounded. First, the Examiner does not specify what the "effective synchronization scheme" is to do – what, precisely, is to be synchronized with what? And in any event, the claims on appeal do not relate to synchronization. Second, it is unclear what is meant by "to function properly." The conclusion that "an effective synchronization scheme" is "require[d]" is therefore meaningless at best.

The Examiner goes on:

> "Secondly, Examiner notes Appellant's concession that the combination of Georgiou and McDermott would indeed yield an improved Georgiou's device based on an improved PLL as taught by McDermott. Examiner agrees that a PLL with a predetermined demanding level input to better control frequency

reduction based on temperature changes is an improvement and provides proper motivation for the combination."

The first sentence of the above mischaracterizes the Appellant's argument. The appeal brief did not argue that "the combination of Georgiou and McDermott would indeed yield an improved Georgiou's device based on an improved PLL," but that "at most the combination of Georgiou with McDermott yields Georgiou's device plus an improved PLL." That is, McDermott's PLL is completely distinct from and irrelevant to Georgiou's device.

The second sentence of the above is simply erroneous. As discussed in the foregoing, the combination of Georgiou et al. and McDermott in no way results in "a PLL with a predetermined demanding level input to better control frequency reduction based on temperature changes ... " for at least the reason that McDermott does not disclose a performance demanding level input for determining a rate of frequency reduction based on a demand for performance at a given level in a processor as called for in the claims on appeal.

Finally, it is observed that the Examiner "submits that PLLs are commonly used in frequency controls such as throttling or frequency reduction, including Appellant's claimed apparatus that also employs a PLL [item 310] in the frequency control process" (Examiner's Answer, page 11, lines 15-18). This supports the Appellant's position, not the Examiner's. The fact that the PLL disclosed in the Appellant's application is distinct from the performance demanding level input is a clear indication that a PLL is not involved with and is irrelevant to the performance demanding level input.

## Conclusion

In view of the above, it is clear that the Examiner erred in finally rejecting claims 1-20. It is therefore respectfully requested that the Board reverse the Examiner and allow claims1-20.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: April 3, 2006 By: _____
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